

What is claimed is:

1. A film bulk acoustic resonator comprising:

5 a semiconductor substrate;

a lower electrode more than two layers formed at an upper surface of the semiconductor substrate;

a piezoelectric layer deposited on an upper surface of the lower electrode;

and

10 an upper electrode more than two layers formed at an upper surface of the piezoelectric layer.

2. The film bulk acoustic resonator of claim 1, wherein the lower electrode or the upper electrode is formed with one pair among Ti/Mo, Cr/Mo, Ti/W,

15 and Cr/W.

3. A duplexer filter comprising:

a semiconductor substrate;

a transmission side film bulk acoustic filter formed at an upper surface of

20 the semiconductor substrate accordingly as a plurality of film bulk acoustic resonators are connected serially and in parallel;

a reception side film bulk acoustic filter formed at one side of the transmission side film bulk acoustic filter accordingly as a plurality of film bulk acoustic resonators are connected serially and in parallel; and

25 a plurality of passive elements formed at one side of the transmission side

film bulk acoustic filter and the reception side film bulk acoustic filter.

4. The duplexer filter of claim 3, further comprising an insulating film between the plurality of film bulk acoustic resonators and the semiconductor substrate.

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5. The duplexer filter of claim 3, further comprising a film bulk acoustic filter for GPS at an upper surface of the semiconductor substrate.

6. A semiconductor package comprising:

10 a semiconductor chip having a transmission side film bulk acoustic filter and a reception side film bulk acoustic filter formed at an upper surface of a semiconductor substrate accordingly as a plurality of film bulk acoustic resonators are connected serially and in parallel;

15 a substrate provided with a ceramic body having a cavity of a certain space so that the semiconductor chip can be mounted, a ground plan formed at a bottom surface of the cavity of the ceramic body, a plurality of conductive ground vias connected to the ground plan for penetrating the ceramic body, and a plurality of signal wires formed from an outer circumference surface of the cavity of the ceramic body to a bottom surface thereof;

20 a plurality of conductive wires for connecting the semiconductor chip, the ground plan, and the signal wires; and

a lid for covering an upper portion of the cavity of the substrate so that the semiconductor chip and the conductive wires can be protected from the external environment.

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7. A semiconductor package comprising:

a semiconductor chip having a transmission side film bulk acoustic filter and a reception side film bulk acoustic filter formed at an upper surface of a semiconductor substrate accordingly as a plurality of film bulk acoustic resonators
5 are connected serially and in parallel;

a substrate provided with a ceramic body where the semiconductor chip is mounted, a plurality of wire patterns formed at an upper surface of the ceramic body so that the semiconductor chip can be connected thereto by a solder as a flip chip form with an overturned state, and a plurality of conductive ground vias and
10 signal conductive vias connected to the plurality of wire patterns and penetrating the ceramic body; and

a sealing layer for sealing the semiconductor chip of the upper surface of the ceramic body for protection from the external environment.

15 8. The semiconductor package of claim 7, further comprising a plurality of passive elements at the semiconductor chip.

9. The semiconductor package of claim 7, wherein the substrate is one selected from a low temperature co-fired ceramic (LTCC) or a high
20 temperature co-fired ceramic (HTCC).

10. The semiconductor package of claim 7, wherein the substrate is an LTCC where a plurality of passive elements are formed, and the plurality of passive elements are formed inside the LTCC.

11. The semiconductor package of claim 7, wherein the sealing layer is one selected from epoxy or polymer.

12. The semiconductor package of claim 7, further comprising an air gap for preventing characteristics of the film bulk acoustic filters formed at a lower surface of the semiconductor chip from being deteriorated between the lower surface of the semiconductor chip and the substrate.

13. A semiconductor package comprising:

a semiconductor chip having a transmission side film bulk acoustic filter and a reception side film bulk acoustic filter formed at an upper surface of a semiconductor substrate accordingly as a plurality of film bulk acoustic resonators are connected serially and in parallel;

a substrate having an insulating body where the semiconductor chip is mounted and having a plurality of wire patterns formed at an upper surface of the insulating body so that the semiconductor chip can be connected thereto by a solder as a flip chip form with an overturned state; and

a sealing layer for sealing the semiconductor chip of the upper surface of the insulating body for protection from the external environment.

14. The semiconductor package of claim 13, wherein the insulating body is one selected from silicon, a printed circuit board, or ceramic having a high resistance.

15. The semiconductor package of claim 13, further comprising a

plurality of passive elements at a region corresponding to the semiconductor chip at an upper surface of the insulating body.

16. The semiconductor package of claim 15, further comprising an air gap for preventing characteristics of the film bulk acoustic filters formed at a lower surface of the semiconductor chip and the passive elements formed at an upper surface of the substrate from being deteriorated between the lower surface of the semiconductor chip and the upper surface of the substrate.

17. The semiconductor package of claim 13, wherein conductive ground vias and a signal conductive via are penetratingly-formed at the insulating body, and the conductive ground vias are connected to the plurality of wire patterns formed at the upper surface of the insulating body.

18. The semiconductor package of claim 13, wherein the plurality of wire patterns formed at the upper surface of the insulating body are extended to outside of the semiconductor chip along the upper surface of the insulating body.